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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/871,596	05/30/2001	Noriyuki Saruhashi	81754.0061	8586

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	9

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/871,596	SARUHASHI ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *2 and 3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. In view of Amendment A of Paper No. 8, the objection to the specification is withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 1-3 have been considered but are moot in view of the new ground(s) of rejection. Note: Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.**

Claim Objections

3. Claims 2 and 3 are objected to because of the following informalities: claim 2 is replete with grammatical and punctuation errors (e.g. in line 5, 'compromising' is incorrectly used; in line 6, double commas are used; in line 13, "connected to a connection" is redundant; etc.). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said test link layer circuit" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Shinozuka, Satoshi (US 6560200 B1).

35 U.S.C. 102(e) rejection of claim 1.

Shinozuka teaches a method for testing a physical layer device including a link layer interface, a physical layer logic circuit to be connected to said link layer interface (The circuit in Figure 1 of Shinozuka clearly provides a method for testing a physical layer device, Serial Bus Experimental Apparatus 2_n, including a link layer interface 5_n and a physical layer logic circuit 4_n connected to said link layer interface 5_n), and a plurality of

ports to be connected to said physical layer logic circuit (Figure 6 in Shinozuka teaches that a plurality of ports are connected to any physical layer logic circuit 4_i through High Performance Serial Bus 1 and Serial Bus Cables 1_i) are provided beforehand in said physical layer device (Packet Capture Circuit 32 in Figure 1 of Shinozuka is part of the physical layer device, Serial Bus Experimental Apparatus 2_n; Note: Merriam-Webster's Dictionary defines beforehand as in advance or ahead of time and since the circuitry with corresponding connections are in place before testing starts, the circuitry with corresponding connections are provided beforehand in said physical layer device); in testing, said test link layer circuit (Packet Capture Circuit 32 in Figure 1 of Shinozuka) is connected to said physical layer logic circuit (physical layer logic circuit 4_n) through said link layer interface (link layer interface 5_n), and said test physical layer logic circuit (Packet Capture Circuit 32 in Figure 1 of Shinozuka) is connected to a first port (1_{n-1} in Figure 6 of Shinozuka; Note: the test physical layer logic circuit Packet Capture Circuit 32 is connected to port 1_{n-1} via physical layer logic circuit 4_n) that is one of said plurality of ports and said first port (1_{n-1} in Figure 6 of Shinozuka) is connected to a second port (1_i in Figure 6 of Shinozuka) that is one of said Plurality of ports through an external bus (1 in Figure 6 of Shinozuka) and the second port (1_i in Figure 6 of Shinozuka) is connected to said physical layer logic circuit (physical layer logic circuit 4_n; Note: physical layer logic circuit 4_n is connected to the second port 1_i via High Performance Serial Bus 1 in Figure 6); and said link layer interface, said physical layer logic circuit, and said plurality of ports are tested (col.2, lines 14-30, Shinozuka).

35 U.S.C. 102(e) rejection of claim 2.

Shinozuka teaches a physical layer device with test circuits, said physical layer device including a link layer interface, a physical layer logic circuit to be connected to said link layer interface (Serial Bus Experimental Apparatus 2_n in Figure 1 of Shinozuka includes a link layer interface 5_n, a physical layer logic circuit 4_n connected to said link layer interface, hence is a physical layer device with test circuits), and a plurality of ports to be connected to said physical layer logic circuit (Figure 6 in Shinozuka teaches that a plurality of ports are connected to any physical layer logic circuit 4_i through High Performance Serial Bus 1 and Serial Bus Cables 1_i), said physical layer device characterized by comprising: a test link layer circuit (Packet Capture Circuit 32 in Figure 1 of Shinozuka is a test link layer circuit) for establishing, in testing, a connection with said link layer interface (link layer interface 5_n; Note: Packet Capture Circuit 32 in Figure 1 of Shinozuka is physically connected to link layer interface 5_n so that anytime test data is communicated via link layer interface 5_n, a connection is established), a connection with said physical layer logic circuit (physical layer logic circuit 4_n) through said link layer interface (link layer interface 5_n) and communicating predetermined data with said physical layer logic circuit (physical layer logic circuit 4_n); and a test physical layer logic circuit (test link layer circuit Packet Capture Circuit 32 in Figure 1 of Shinozuka) for establishing, in testing, a connection with said plurality of ports, wherein a first port that is one of said plurality of ports (1_{n-1} in Figure 6 of Shinozuka is a first test port; Note: the test physical layer logic circuit Packet Capture Circuit 32 is connected to port 1_{n-1} via physical layer logic circuit 4_n), is connected to a second port (1_i in Figure 6 of

Shinozuka) that is one of said plurality of ports through an external bus (Serial Bus 1 in Figure 6), where the first (1_{n-1} in Figure 6 of Shinozuka) and second ports (1_i in Figure 6 of Shinozuka) are connected to a connection (High Performance Serial Bus 1) with said physical layer logic circuit (physical layer logic circuit 4_n) through said plurality of ports and communicating predetermined data with said physical layer logic circuit (physical layer logic circuit 4_n).

35 U.S.C. 102(e) rejection of claim 3.

Each Node Instrument 2_i in Figure 6 has a control means for establishing a connection with an external link layer device or said test link layer circuit or for selectively establishing a connection with said physical layer logic circuit or said test physical layer logic circuit, hence the control means 3_i in Figure 6 are a switching means.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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